Bias–Dependent "Cold–(H)FET" Modeling

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Abstract

A bias–dependent model for MESFET and HFET devices under zero drain bias pinched–off conditions is proposed. Parasitic capacitances are evaluated from bias–dependent Y parameters over the whole frequency range. For the first time, it is possible to clearly distinguish between all intrinsic and extrinsic capacitances by considering the distributed nature of the device.

Introduction

The accurate determination of the FET's parasitics becomes increasingly important in the degree the operating frequencies extent and the chip size of the intrinsic device reduces compared with the pad size [5]. To determine the parasitics it is common practise to consider the "Cold–(H)FET" which stands for a FET/HFET operating at zero drain–source voltage. In this case, the intrinsic transistor can be understood as symmetrically regarding the gate–metalization. Therefore, this device can be described by an equivalent circuit with a significantly reduced number of elements and parameters, respectively [1], [2], [3], [4]. To particularly determine the parasitic capacitances the gate–source voltage is reverse–biased beyond the pinch–off voltage, causing a fully depleted region under the gate. Since the intrinsic transistor is symmetrically, the equivalent circuit has only two independent parameters. Up to now it was not possible to distinguish between the intrinsic drain–source capacitance and the extrinsic– or pad–capacitance at the drain. The proposed model describes the bias-dependence of the depletion layer's equivalent circuit and leads to physically meaningful, i.e. bias–*in*dependent, extrinsic capacitances. It has been common practise to use only low frequency Y parameters to determine the capacitances. In our model short transmission lines take account of the distributed nature of the pad–structure. This leads to a frequency–independent gradient of the imaginary part of the intrinsic Y parameters over the full measured frequency range and allows to distinguish between the parasitic effects of the feeding structure and the parasitics of the transistor cell.

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Model and Parameter Extraction

Figure 1 shows the equivalent circuit of a pinched–off "Cold–(H)FET" with two transmission lines (TRL) which model the grounded coplanar feeding structure. The physical origin of the equivalent circuit elements is indicated in figure 2 by means of a schematic cross section.

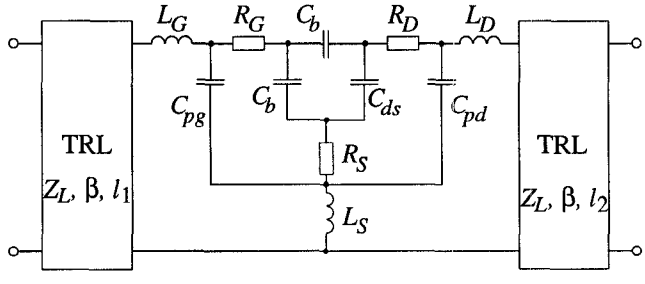

Fig. 1. Equivalent Circuit of a pinched–off "Cold–(H)FET" with transmission lines (TRL).

A. Transmission Lines

From a typical layout of a MESFET/HFET for MMIC applications it can clearly be seen that the coplanar feeding structure contributes decisively to the reactive parasitics. The parameters of the transmission line (Z_L and $\epsilon_{r,\mathrm{eff}}$) can be calculated (e.g. [6]) since the layout dimensions and the technology data are well known. To eliminate the

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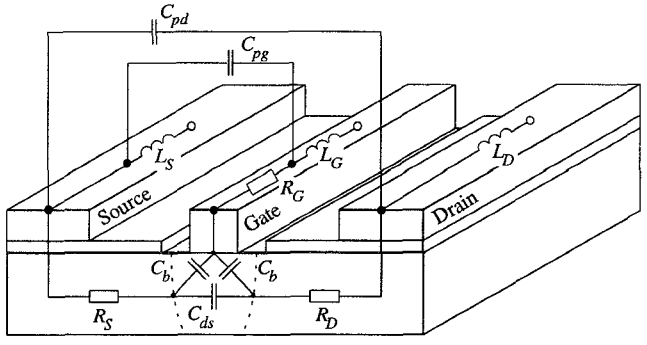

Fig. 2. Schematic cross section of a pinched–off "Cold–(H)FET" showing the physical origin of the equivalent circuit elements. (Airbridges are not depicted to keep the figure clearly arranged.)

effect of the TRLs on the measured data we convert them into chain matrices and multiply by the inverted chain matrices of the TRLs on both sides. The result can be converted into Y parameters for the following deembedding procedure.

$$\begin{aligned} \boldsymbol{S}_{\text{meas}} &\longrightarrow \boldsymbol{A}_{\text{meas}} \\ \boldsymbol{A}_{\text{FET}} &= \boldsymbol{A}_{\text{TRL}_1}{}^{-1} \cdot \boldsymbol{A}_{\text{meas}} \cdot \boldsymbol{A}_{\text{TRL}_2}{}^{-1} \quad (1) \\ \boldsymbol{A}_{\text{FET}} &\longrightarrow \boldsymbol{Y}_{\text{FET}} \end{aligned}$$

whereby the inverse chain matrix of the TRL is given by

$$\boldsymbol{A}_{\text{TRL}}^{-1} = \begin{pmatrix} \cos\beta l & -\mathrm{j}\, Z_L \sin\beta l \\ -\mathrm{j}\, Z_L{}^{-1} \sin\beta l & \cos\beta l \end{pmatrix} \quad (2)$$

This procedure leads to a frequency–independent gradient of the imaginary part of the FET's intrinsic Y parameters over the full frequency range. We determine both lengths $l_{1,2}$ by minimizing the frequency dependence of the pinched–off "Cold–FET's" intrinsic capacitances. (The starting values are the physical length of the transmission lines which are given by the layout.) The validity of the approach is verified by determining the lengths for different gate–source voltages. The extracted lengths show nearly no gate–source voltage dependence despite of the considerably variation of the intrinsic capacitances.

For a state–of–the–art GaAlAs/GaAs–HFET, the dimension of which can be one order of magnitude larger than the intrinsic device, the feeding lines represent roughly 90% of the total inductance of the device. Consequently, the consideration of the TRLs is leading to much better results concerning the remaining capacitive circuit elements.

B. Intrinsic "Cold–FET" Model

Under the common presumption, that the parasitic and the intrinsic capacitances can be summarized, the capacitive circuit elements are evaluated by determining the gradient of the imaginary part of the Y parameters against frequency[1]. The imaginary part of the Y matrix corresponding to the equivalent circuit is given by

$$Im\{\boldsymbol{Y}_{\text{FET}}\} = \omega \begin{pmatrix} (C_{pg} + 2\,C_b) & -C_b \\ -C_b & (C_{pd} + C_b + C_{ds}) \end{pmatrix} \quad (3)$$

Our new approach models the region beneath the gate of a pinched–off "Cold–(H)FET" by means of a uniform, capacitive transmission line (see fig. 3).

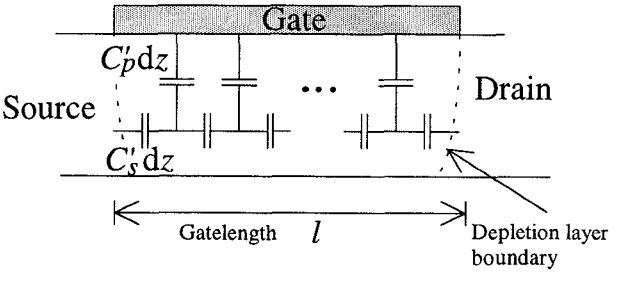

Fig. 3. Schematic cross section of the region beneath the gate of a pinched–off "Cold–(H)FET" with an uniform, capacitive transmission line model in the region of the depletion layer.

Each infinitesimal short transmission line element of length $\mathrm{d}z$ consists of a capacitance in series ($C_s'\mathrm{d}z$) and in parallel ($C_p'\mathrm{d}z$). The Y parameters of such a transmission line of the length l are given by

$$\boldsymbol{Y} = \frac{1}{Z_L \sinh(\gamma l)} \begin{pmatrix} \cosh(\gamma l) & -1 \\ -1 & \cosh(\gamma l) \end{pmatrix} \quad (4)$$

where

$$Z_L = \left(\mathrm{j}\omega\sqrt{C_s'\, C_p'}\right)^{-1} \quad \text{and} \quad \gamma = \sqrt{C_p'/C_s'} \quad (5)$$

[1]As for the resistances it would be necessary to determine the gradient of the Z parameters resulting in a "T"–equivalent circuit which is then converted into a "π"–equivalent circuit; but measurement results show that both procedures lead to nearly identical results.

yielding the intrinsic circuit elements

$$C_b = \frac{\cosh(\gamma l) - 1}{Z_L \sinh(\gamma l)} \quad (6)$$

$$C_{ds} = \frac{1}{Z_L \sinh(\gamma l)} \quad (7)$$

During the extraction procedure it is convenient to consider a measured, capacitive "π"–equivalent circuit

$$C_{1\pi} = \frac{1}{\omega} Im\{Y_{11} + Y_{12}\}_{\mathrm{FET}} \quad (8)$$

$$C_{2\pi} = \frac{1}{\omega} Im\{-Y_{12}\}_{\mathrm{FET}} \quad (9)$$

$$C_{3\pi} = \frac{1}{\omega} Im\{Y_{22} + Y_{12}\}_{\mathrm{FET}} \quad (10)$$

With equations (3), (6) .. (10) it can readily be shown, that the extrinsic capacitances are given by

$$C_{pg} = C_{1\pi} - C_{2\pi} \quad (11)$$

$$C_{pd} = C_{3\pi} - \frac{C_{2\pi}}{\cosh(\gamma l) - 1} \quad (12)$$

Eq. (11) is the result of previous work but eq. (12) represents a totaly new approach (see table I).

author	C_{pg}	C_{pd}
Dambrine [1]	$C_{1\pi} - C_{2\pi}$	$C_{3\pi}$
White [2]	$C_{1\pi} - C_{2\pi}$	$C_{3\pi} - C_{2\pi}$
this paper	$C_{1\pi} - C_{2\pi}$	$C_{3\pi} - \frac{C_{2\pi}}{(\cosh(\gamma l)-1)}$

TABLE I

Since the physical length of the depletion layer varies with the applied gate–source voltage we use a first order approach to model the gate–source voltage–dependence of the length l.

$$l = \alpha(V_0 - V_{GS}) \quad (13)$$

To determine the parasitic capacitance C_{pd} we transform eq. (12) with the linear model of eq. (13), yielding ($\alpha' = \gamma\alpha$)

$$\operatorname{arcosh}\left(\frac{C_{2\pi}}{C_{3\pi} - C_{pd}} + 1\right) = \alpha' \, (V_0 - V_{GS}) \quad (14)$$

The capacitances $C_{i\pi}$ (i=2,3) are known by measurement. C_{pd} is given by the value which minimizes eq. (14) by means of a modified linear regression.

Measurements/Results

The bias–dependent S parameters of many "Cold–PMHFETs" ($l_G = 0.25\mu$m, $w_G = 4 \times 45\mu$m) were measured with a Wiltron 360B ANA in the frequency range of $f = 40$ MHz to 40 GHz. Figure 4 shows the effect of considering the TRLs on the imaginary part of Y_{11}.

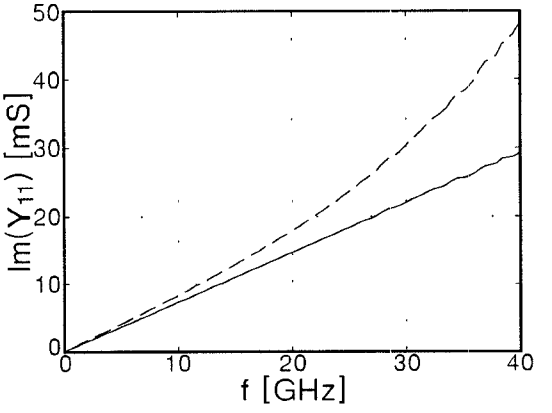

Fig. 4. Imaginary part of Y_{11} vs. frequency: (- - -) disregarding TRLs during the extraction procedure, (—) with TRLs.

Figure 5 shows the extracted capacitance C_{pd}, and C_{ds} versus the gate–source voltage according to eq.(12). The value of C_{pd} remains constant throughout the full voltage range. The intrinsic capacitance C_{ds} increases with the gate–source voltage approaching the pinch–off voltage and zero length, respectively. To demonstrate the validity of the approach to use a first order model for the depletion layer length variation, we show the transformed data according to eq.(14). Finally, we present the bias–dependent parameter S_{11} at 40 GHz (fig. 7) to show the good agreement of measured and modeled data.

Conclusion

A bias–dependent model for MESFET and HFET devices under zero drain bias pinched–off conditions along with the parameter extraction procedure

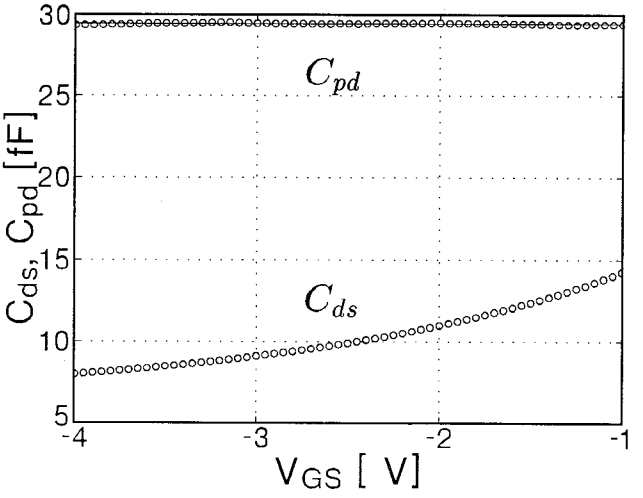

Fig. 5. Extracted capacitances C_{pd} and C_{ds} vs. gate–source voltage V_{GS}

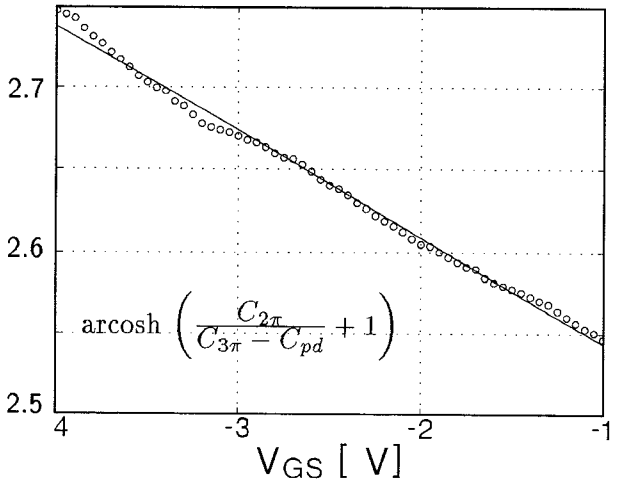

Fig. 6. According to eq.(14) transformed data vs. gate–source voltage demonstrating the validity of the approach to use a first order model.

is proposed. The introduction of transmission lines for the extrinsic coplanar feeding structure and a uniform capacitive transmission line approach for the V_{GS} dependence of the depletion layer beneath the gate lead to significant improvements of the "Cold–FET" model:

1. Frequency independence of the capacitances.
2. Capability to distinguish between the intrinsic and extrinsic part of the drain–source capacitance.
3. Bias–independence of the extrinsic capacitance C_{pd}.

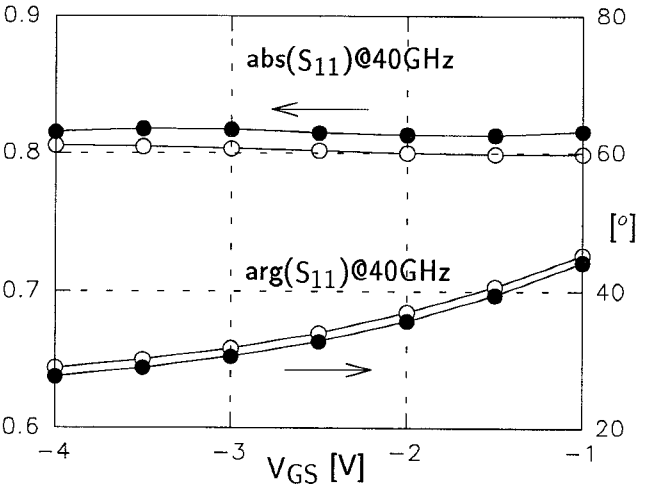

Fig. 7. Magnitude and Phase of S_{11} at 40 GHz vs. the gate–source voltage, (•) measured, (o) modeled.

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